



FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

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APPLICANT(S): Hammond *et al.*

SERIAL NO.: 10/688,003

FILING DATE: October 17, 2003

GROUP: ~~Not yet assigned~~ 2811

## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
JH	A1	4,908,681	03/13/1990	Nishida <i>et al.</i>	—	—	
	A2	5,534,713 ✓	07/09/1996	Ismail <i>et al.</i>	—	—	
	A3	5,557,231	09/17/1996	Yamaguchi <i>et al.</i>	—	—	
	A4	5,672,995	09/30/1997	Hirase <i>et al.</i>	—	—	
	A5	5,692,002	11/25/1997	Mizutani	—	—	
	A6	5,877,056	03/02/1999	Wu <i>et al.</i>	—	—	
	A7	6,040,208	03/21/2000	Honeycutt <i>et al.</i>	—	—	
	A8	6,284,615	09/04/2001	Pinto <i>et al.</i>	—	—	
	A9	6,310,367	10/30/2001	Yagishita <i>et al.</i>	—	—	
	A10	6,313,016	11/06/2001	Kibbel <i>et al.</i>	—	—	
	A11	6,448,840	09/10/2002	Kao <i>et al.</i>	—	—	
JH	A12	6,680,496	01/20/2004	Hammond <i>et al.</i>	257	192	07/08/2002

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
JH	C1	Burd <i>et al.</i> , "A Dynamic Voltage Scaled Microprocessor System," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11 (November 2000), pp. 1571-1580.							
	C2	Gonzalez <i>et al.</i> , "Supply and Threshold Voltage Scaling for Low Power CMOS," IEEE Journal of Solid-State Circuits, Vol. 32, No. 8 (August 1997), pp. 1210-1216.							
	C3	Miyazaki <i>et al.</i> , "A Delay Distribution Squeezing Scheme with Speed-Adaptive Threshold-Voltage CMOS (SA-Vt CMOS) for Low Voltage LSIs," ISLPED'98 (International Symposium on Low Power Electronics and Design), pp. 48-53.							
JH	C4	von Kaenel <i>et al.</i> , "Automatic Adjustment of Threshold & Supply Voltages for Minimum Power Consumption in CMOS Digital Circuits," IEEE Symposium on Low Power Electronics (1994), pps. 78-79.							

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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>SKM</i>	A13	2002/0008289	01/24/2002	Murota <i>et al.</i>			
<i>SKM</i>	A14	2002/0030203	03/14/2002	Fitzgerald			
	<del>A15</del>	<del>2002/0104993</del>	<del>08/08/2002</del>	<del>Fitzgerald <i>et al.</i></del>			
	<del>A16</del>	<del>2002/0123167</del>	<del>09/05/2002</del>	<del>Fitzgerald</del>			
	<del>A17</del>	<del>2002/0123183</del>	<del>09/05/2002</del>	<del>Fitzgerald</del>			
	<del>A18</del>	<del>2002/0125497</del>	<del>09/12/2002</del>	<del>Fitzgerald</del>			
	A19	2003/0013323	01/16/2003	Hammond <i>et al.</i>			
	<del>A20</del>	<del>2003/0052406</del>	<del>03/20/2003</del>	<del>Lochtefeld <i>et al.</i></del>			
	<del>A21</del>	<del>2003/0077867</del>	<del>04/24/2003</del>	<del>Fitzgerald</del>			
	<del>A22</del>	<del>2003/0102498</del>	<del>06/05/2003</del>	<del>Draithwaite <i>et al.</i></del>			
	<del>A23</del>	<del>2003/0207571</del>	<del>11/06/2003</del>	<del>Fitzgerald <i>et al.</i></del>			04/23/2003
<i>SKM</i>	A24	4,212,019	07/08/1980	Wataze <i>et al.</i>			
	A25	4,771,013	09/13/1988	Curran			
	A26	5,101,254	03/31/1992	Hamana			
	A27	5,244,749	09/14/1993	Bean <i>et al.</i>			
	A28	5,331,185	07/19/1994	Kuwata			
	A29	5,461,245	10/24/1995	Gribnikov <i>et al.</i>			
	A30	5,548,138	08/20/1996	Tanimoto <i>et al.</i>			
	A31	5,739,567	04/14/1998	Wong			
	A32	5,780,922	07/14/1998	Mishra <i>et al.</i>			
	A33	5,789,799	08/04/1998	Voinigescu <i>et al.</i>			
<i>SKM</i>	A34	5,898,342	04/27/1999	Bell			
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<i>AKM</i>	A35	6,052,380	04/18/2000	Bell	—	—	
	A36	6,111,267 ✓	08/29/2000	Fischer <i>et al.</i>	257	19	
	A37	6,111,367	08/29/2000	Asano <i>et al.</i>	—	—	
	A38	6,140,687	10/31/2000	Shimomura <i>et al.</i>	—	—	
	A39	6,160,274	12/12/2000	Folkes	—	—	
	A40	6,271,726	08/07/2001	Fransis <i>et al.</i>	—	—	
	A41	6,555,839 ✓	04/29/2003	Fitzgerald	257	19	
	A42	6,583,015	06/24/2003	Fitzgerald <i>et al.</i>	—	—	
	A43	6,593,191	07/15/2003	Fitzgerald	—	—	
	A44	6,593,641	07/15/2003	Fitzgerald	—	—	
<i>AKM</i>	A45	6,646,322	11/11/2003	Fitzgerald	—	—	07/16/2001

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	<del>B1</del>	<del>01/933338 A1</del> <i>corresponds to US 6,555,839</i>	<del>12/06/2001</del>	<del>WO</del>				N	Y
	<del>B2</del>	<del>02/43262 A2</del> <i>corresponds to US 6,523,015</i>	<del>02/14/2002</del>	<del>WO</del>				N	Y
	<del>B3</del>	<del>02/071488 A1</del>	<del>09/12/2002</del>	<del>WO</del>				N	Y
	<del>B4</del>	<del>02/071491 A1</del>	<del>09/12/2002</del>	<del>WO</del>				N	Y
	<del>B5</del>	<del>02/071493 A3</del>	<del>09/12/2002</del>	<del>WO</del>				N	Y
	<del>B6</del>	<del>02/071495 A1</del>	<del>09/12/2002</del>	<del>WO</del>				N	Y
	<del>B7</del>	<del>02/403760 A2</del>	<del>12/27/2002</del>	<del>WO</del>				N	Y
	<del>B8</del>	<del>03/015138 A2</del>	<del>02/20/2003</del>	<del>WO</del>				N	Y

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OTHER ART, JOURNAL ARTICLES, ETC.			
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)		
<i>SKM</i>	C5	Abidi <i>et al.</i> , "Power-Conscious Design of Wireless Circuits and Systems," <u>IEEE-2000</u> , Vol. 88, Issue 10 (October 2000), pp. 1528-1545.	
	C6	Abou-Allam <i>et al.</i> , "Impact of Technology Scaling on CMOS RF Devices and Circuits," <u>IEEE 2000 Custom Integration Circuits Conference</u> , (2000), pp. 361-364.	
	C7	Aniel <i>et al.</i> , "Low Temperature Analysis of 0.25 $\mu$ m T-Gate Strained Si/Si0.55Ge0.45 N-MODFET's," <u>IEEE</u> , Vol. 47, Issue 7 (July 2000), pp. 1477-1483.	
<i>SKM</i>	C8	Ansley <i>et al.</i> , "Based Profile Optimization for Minimum Noise Figure in Advanced UHV/CVD SiGe HBTs," <u>IEEE Transactions on Microwave Theory and Techniques</u> , Vol. 46, No. 5 (May 1998), pp. 653-660.	
	<del>C9</del>	<del>Armstrong <i>et al.</i>, "Technology for SiGe Heterostructure-Based CMOS Device," PhD Thesis, Massachusetts Institute of Technology, 1999, pp. 1-154.</del>	
<i>SKM</i>	C10	Assaderaghi <i>et al.</i> , "Current Status of Technology, Modeling, Design, and the Outlook for the 0.1 $\mu$ m Generation," <u>IEEE International SOI Conference 2000</u> , (October 2000), pp. 6-9.	
	C11	Borovitskaya <i>et al.</i> , "On Theory of 1/F Noise in Semiconductors," <u>Solid-State Electronics</u> , Vol. 45, Issue 7 (July 2001), pp. 1067-1069.	
	C12	Brouk <i>et al.</i> , "Dimensional Effects in CMOS Photodiodes," <u>Solid-State Electronics</u> , Vol. 46, Issue 1 (January 2002), pp. 19-28.	
	C13	Chatterjee <i>et al.</i> , "SUM-100NM Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process," <u>IEEE</u> , (1997), pp. 1-4.	
	C14	Chen <i>et al.</i> , "High-Performance Fully-Depleted SOI RF CMOS," <u>IEEE Electron Device Letters</u> , Vol. 23, Issue 1 (January 2002), pp. 52-54.	
	C15	Chen <i>et al.</i> , "Impact of Intrinsic Channel Resistance on Noise Performance of CMOS LNA," <u>IEEE Electron Device Letters</u> , Vol. 23, Issue 1 (January 2002), pp. 34-36.	
	C16	Chew <i>et al.</i> , "Driving CMOS into the Wireless Communications Arena with Technology Scaling," <u>IEEE 2001 Custom Integrated Circuits Conference</u> , (2001), pp. 571-574.	
	C17	Choi <i>et al.</i> , "A Low Noise On-Chip Matched MMIC LNA of 0.76DB Noise Figure at 5 GHz for High Speed Wireless LAN Applications," <u>IEEE - GaAs IC Symposium</u> , (2000), pp. 143-146.	
	C18	Choi <i>et al.</i> , "Low Noise PHEMT and its MMIC LNA Implementation for C-Band Applications," <u>IEEE 2000 Conference on Microwave and Millimeter Wave Technology Proceedings</u> , (2000), pp. 56-59.	
	C19	Cressler <i>et al.</i> , "SiGe HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications," <u>IEEE Transactions on Microwave Theory and Techniques</u> , Vol. 46, Issue 5 (May 1998), pp. 572-589.	
	C20	Cressler <i>et al.</i> , "Silicon-Germanium Heterojunction Bipolar Technology: The Next Leap in Silicon?" <u>IEEE International Solid-State Circuits Technology</u> , (1994), pp. 24-27.	
<i>SKM</i>	C21	Enciso-Aguilar <i>et al.</i> , "De-Embedded Ultra-Low Noise 0.1 $\mu$ m Gate Length Ge/Si0.4Ge0.6 P-Modfet," <u>IEEE - Electron Device Letters</u> , Vol. 37, Issue 24 (November 22, 2001), pp. 1478-1479.	
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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)		
<i>SKM</i>	C22	Enciso-Aguilar <i>et al.</i> , "0.3DB Minimum Noise Figure at 25 GHz of 0.13 $\mu$ M Si/Si <sub>0.58</sub> Ge <sub>0.42</sub> N-MODFETS," <u>IEEE - Electron Device Letters</u> , Vol. 37, Issue 17 (August 16, 2001), pp. 1089-1090.	
	C23	Fobelets <i>et al.</i> , "Si: SiGe Modfet Current Mirror," <u>IEEE Electron Device Letters</u> , Vol. 34, Issue 22 (October 29, 1998), pp. 2076-2077.	
	C24	Frank <i>et al.</i> , "Device Scaling Limits of Si MOSFETS and their Application Dependencies," <u>IEEE Proceedings</u> , Vol. 89, Issue 3 (March 2001), pp. 259-288.	
	C25	Gilbert <i>et al.</i> , "Analog at Milepost 2000: A Personal Perspective," <u>IEEE-2001</u> , Vol. 89, Issue 3 (March 2001), pp. 289-304.	
	C26	Gray <i>et al.</i> , "Analysis and Design of Analog Integrated Circuits," John Wiley & Sons Publishing Co., Second Edition (1984), pp. 604-688.	
	C27	Haramé <i>et al.</i> , "Optimization of SiGe HBT Technology for High Speed Analog and Mixed Signal Applications," <u>IEEE-IEDM 93 Conference</u> , (December 1993), pp. 71-73.	
	C28	Haramé <i>et al.</i> , "Si/SiGe Epitaxial-Base Transistors Part II: Process Integration and Analog Applications," <u>IEEE Transactions on Electron Devices</u> , Vol. 42, Issue 3 (March 1995), pp. 469-482.	
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	C30	Huang <i>et al.</i> , "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits," <u>IEEE Journal of Solid State Circuits</u> , Vol. 33, Issue 7 (July 1998), pp. 1023-1036.	
	C31	Jain <i>et al.</i> , "SiGe HBT for Application in Bicmos Technology II: Design, Technology and Performance," <u>Semiconductor Science and Technology</u> , Vol. 16 (July 2001), pp. R67-R85.	
	C32	Kar <i>et al.</i> , "Estimation of Hole Mobility in Strained Si <sub>1-x</sub> Ge <sub>x</sub> Buried Channel Heterostructure PMOSFET," <u>Solid State Electronics</u> , Vol. 45, Issue 5 (May 2001), pp. 669-676.	
	C33	Kim <i>et al.</i> , "A Fully Integrated 1.9GHz CMOS Low-Noise Amplifier," <u>IEEE Microwave and Guided Wave Letters</u> , Vol. 8, Issue 8 (August 1998), pp. 293-295.	
	C34	Kim <i>et al.</i> , "Novel RF Isolation Structures Using Porous Si," University of California, Los Angeles, CA, (2000), pp. 1-11.	
	C35	Klepser <i>et al.</i> , "A 10 GHz SiGe BiCMOS Phase-Locked-Loop Frequency Synthesizer," <u>IEEE 2001 Custom Integrated Circuits Conference</u> , (July 2001), pp. 567-570.	
	C36	Koester <i>et al.</i> , "SiGe PMODFETs on Silicon-on-Sapphire Substrates with 116 GHz FMAX," <u>IEEE Electron Device Letters</u> , Vol. 22, Issue 2 (February 2001), pp. 92-94.	
	C37	Konig <i>et al.</i> , "SiGe HBTs and HFETs," <u>Solid-State Electronics</u> , Vol. 38, Issue 9 (September 1995), pp. 1595-1602.	
	C38	Kumar <i>et al.</i> , "A SOI/CMOS/BJT Technology for Integrated Power Amplifiers Used in Wireless Transceiver Applications," <u>IEEE Electron Device Letters</u> , Vol. 22, Issue 3 (March 2001), pp. 136-138.	
<i>SKM</i>	C39	Kumar <i>et al.</i> , "Novel Isolation Structures for TFSOI Technology," <u>IEEE Electron Device Letters</u> , Vol. 22, Issue 9 (September 2001), pp. 435-437.	
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<i>JKH</i>	C40	Lagnado <i>et al.</i> , "RF Systems Based on Silicon-on-Sapphire Technology," <u>IEEE - 2000 International SOI Conference</u> , (October 2000), pp. 32-33.	
	C41	Lagnado <i>et al.</i> , "Silicon-on-Sapphire for RF Si Systems 2000" <u>IEEE - 2000 Topical Meeting on Digest of Papers</u> , (2000), pp. 79-82.	
	C42	Lambert <i>et al.</i> , "Low Frequency Noise Measurements of P-Channel Si1-xGex Mosfets," <u>IEEE Transactions on Electron Devices</u> , Vol. 46, Issue 7 (July 1999), pp. 1484-1486.	
	C43	Larson <i>et al.</i> , "Integrated Circuit Technology Options for RFIC's - Present Status and Future Directions," <u>IEEE Journal of Solid-State Circuits</u> , Vol. 33, Issue 3 (March 1998), pp. 387-399.	
	C44	Larson <i>et al.</i> , "Manufacturing Study of Yield and Performance Dependence on Gate Length for Submicron Anias-Gainas HEMT's," <u>IEEE Transactions on Semiconductor Manufacturing</u> , Vol. 6, No. 4 (November 1993), pp. 380-383.	
	C45	Lee <i>et al.</i> , "CMOS RF Integrated Circuits at 5 GHz and Beyond," <u>IEEE Proceedings</u> , Vol. 88, Issue 10 (October 2000), pp. 1560-1571.	
	C46	Lee <i>et al.</i> , "Strained Ge Channel P-Type Metal Oxide Semiconductor Field-Effect Transistors Grown in Si1-xGex/Si," <u>Applied Physics Letters</u> , Vol. 79, Issue 20 (November 12, 2001), pp. 3344-3346.	
	C47	Leitz <i>et al.</i> , "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," <u>Materials Research Society Symposium</u> , Vol. 686 (2002), pp. A3.10.1-A3.10.6.	
	C48	Leitz <i>et al.</i> , "Hole Mobility Enhancements in Strained Si/Si1-yGey P-type Metal-Oxide-Semiconductor Field-Effect Transistors Grown on Relaxed Si1-xGe (x<y) Virtual Substrates," <u>Applied Physics Letters</u> , Vol. 79, Issue 25 (December 17, 2001), pp. 4246-4248.	
	C49	Li <i>et al.</i> , "A Comparison of CMOS and SiGe LNA's and Mixers for Wireless LAN Applications," <u>IEEE 2001 Custom Integrated Circuits Conference</u> , (2001), pp. 531-534.	
	C50	Lu <i>et al.</i> , "High Performance 0.15 $\mu$ M Gate-Length P-Type SiGe MODFET's and MOS-MODFET's," <u>IEEE Transactions on Electron Device</u> , Vol. 47, Issue 8 (August 2000), pp. 1645-1652.	
	C51	Lukyanchikova <i>et al.</i> , "Noise Investigation of SiGe and Si nMOSFET's with Gate Oxide Grown by Low Temperature Plasma Anodisation," <u>IEEE - 2000 High Performance Electron Devices for Microwave and Optoelectronic Applications</u> , (2000), pp. 14-19.	
	C52	Maeda <i>et al.</i> , "Feasibility of 0.18 $\mu$ M SOI CMOS Technology Using Hybrid Trench Isolation with High Resistivity Substrate for Embedded RF/Analog Applications," <u>IEEE Transactions on Electron Devices</u> , Vol. 48, Issue 9 (September 2001), pp. 2065-2073.	
	C53	Manku <i>et al.</i> , "Microwave CMOS - Devices and Circuits," <u>IEEE 1998 Custom Integrated Circuits Conference</u> , (May 1998), pp. 59-66.	
	C54	Manku <i>et al.</i> , "RF Simulations and Physics of the Channel Noise Parameters Within MOS Transistors," <u>IEEE 1999 Custom Integrated Circuits Conference</u> , (May 1999), pp. 369-372.	
<i>JKH</i>	C55	Mathew <i>et al.</i> , "Effect of Ge Profile on the Frequency Response of SiGe pFET on Sapphire Technology," Office of Naval Research and IBM Research Division, pp. 130-131.	
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	C57	Michelakis <i>et al.</i> , "SiGe H MOSFET Differential Pair," <u>IEEE-2001 Circuits and Systems - ISCAS International Symposium</u> , (2001), pp. 1679-1682.	
	C58	Momose <i>et al.</i> , "Ultrathin Gate Oxide CMOS with Nondoped Selective Epitaxial Si Channel Layer," <u>IEEE Transactions on Electron Devices</u> , Vol. 48, Issue 6 (June 2001), pp. 1136-1144.	
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	C60	Nishi <i>et al.</i> , "Impact of New Materials, Changes in Physics and Continued ULSI Scaling on Failure Mechanisms and Analysis," <u>IEEE 1999 7th IPFA '99 Singapore</u> , (August 1999), pp. 1-8.	
	C61	Niu <i>et al.</i> , "Noise Modeling and SiGe Profile Design Tradeoffs for RF Applications," <u>IEEE Transactions on Electron Devices</u> , Vol. 47, Issue 11 (November 2000), pp. 2037-2044.	
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	C64	Ohmi <i>et al.</i> , "New Paradigm of Silicon Technology," <u>IEEE Proceedings</u> , Vol. 89, Issue 3 (March 2001), pp. 394-412.	
	C65	Okhonin <i>et al.</i> , "DC and Low-Frequency Noise Characteristics of SiGe P-Channel FET's Designed for 0.13- $\mu$ M Technology," <u>IEEE Transactions on Electron Devices</u> , Vol. 46, Issue 7 (July 1999), pp. 1514-1517.	
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	C69	Pavlidis <i>et al.</i> , "HBT vs. MESFET: What's Best and Why," <u>GaAs Mantech</u> , (1999), pp. 1-4.	
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